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Methods of Forming Transistor Devices

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Methods of Forming Transistor Devices

TECHNICAL FIELD

[0001] The invention pertains to methods of forming transistor devices for semiconductor constructions.

BACKGROUND OF THE INVENTION

[0002] There are numerous applications for transistor devices in semiconductor constructions. For instance, transistor devices can be incorporated into memory array constructions, as well as into logic constructions.

[0003] A typical transistor device will comprise a transistor gate over a semiconductor substrate. The transistor gate will comprise a conductive material, such as, for example, conductively doped polysilicon, and can further comprise metal silicide and/or metal over the conductively doped silicon. The transistor gate will be separated from the semiconductive material substrate by a thin layer of dielectric material. The dielectric material can comprise, for example, silicon dioxide (a so-called gate oxide). Alternatively, the dielectric material can comprise a combination of silicon dioxide and a nitrogen-containing layer formed over the silicon dioxide. The nitrogen-containing layer can be provided to alleviate or prevent dopant diffusion from the conductively-doped silicon of the transistor gate to the underlying semiconductive material substrate, such as, for example, to prevent diffusion of boron.

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[0004] One exemplary method of forming the nitrogen-containing layer of the dielectric material is to expose an underlying silicon dioxide material to activated nitrogen. The activated nitrogen can be formed by exposing a nitrogen precursor (such as, for example, N_2) to a plasma generated at a power which is less than 1,500 watts, for a processing time of no greater than 20 seconds. The relatively low power and processing time duration are utilized because such are found to be sufficient for forming a suitable nitrogen-comprising layer for utilization as a dopant-migration barrier. Accordingly, it would be a waste of energy and processing time to extend the power and the duration of the nitrogen treatment.

[0005] In addition to the gate and dielectric layer discussed above, a transistor device will comprise a channel region within the semiconductor substrate under the transistor gate, and a pair of source/drain regions separated from one another by the channel region. The source/drain regions are selectively electrically connectable through the gate of the transistor device.

[0006] Transistor devices can be divided amongst two broad categories. One type of device comprises n-type conductively doped source/drain regions and is referred to as an NMOS device (with NMOS being an abbreviation for n-type metal-oxide-silicon), and the other type of device comprises p-type conductively doped source/drain regions and is referred to as a PMOS device (with PMOS standing for p-type metal-oxide-silicon). Logic circuitry can comprise combinations of NMOS and PMOS devices in so-called CMOS arrangements.

[0007] Among the difficulties in forming various transistors, and particularly in forming deep sub-micron PMOS transistors, is that the channel region must generally be doped with a threshold voltage (V_t) adjustment implant, to a concentration greater than 7×10^{17} atoms/cm^3 to achieve a reasonable V_t value. It would be desirable to lower the V_t implant concentration, as lower dopant concentrations in a PMOS channel can lead to higher drive currents for the channel, higher mobility within the channel, and lower source and drain junction capacitance. Further, the lower junction capacitance can result in lower source and drain junction leakage within a device.

SUMMARY OF THE INVENTION

[0008] In one aspect, the invention encompasses a method of forming a transistor device. A semiconductor substrate is provided. The substrate has a silicon-comprising surface. The silicon-comprising surface is exposed to activated nitrogen for a time of at least about 20 seconds to convert the silicon-comprising surface to a material comprising silicon and nitrogen. The activated nitrogen is formed by exposing a nitrogen-containing precursor to a plasma generated at a power of at least about 1,500 watts. A transistor gate structure is formed over the material comprising silicon and nitrogen. The transistor gate structure defines a channel region underlying it. The material comprising silicon and nitrogen separates the transistor gate structure from the channel region. A pair of source/drain regions are formed which are separated from one another by the channel region. The material comprising silicon and

nitrogen preferably contains a peak nitrogen concentration of at least about 15 atom %.

[0009] In another aspect, the invention encompasses a method of forming a plurality of transistor devices. A semiconductor substrate having a silicon-comprising surface is provided. A plurality of transistor device channel region locations are defined beneath the silicon-comprising surface. The channel region locations are divided amongst two defined groups, with one of the defined groups being a first group and the other being a second group. The silicon-comprising surface over the second group of transistor device channel region locations is covered with a masking material. The silicon-comprising surface over the first group of transistor device channel region locations is exposed to activated nitrogen for a time of at least about 20 seconds to convert the silicon-comprising surface to a material comprising silicon and nitrogen. The masking material remains over the second group of transistor device channel region locations while the silicon-comprising surface over the first group of transistor device channel region locations is exposed to the activated nitrogen. Subsequently, the masking material is removed and transistor gate structures are formed over the groups of transistor device channel region locations. A plurality of source/drain regions are formed, with individual pairs of the source/drain regions being separated from one another by individual channel region locations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

[0011] Fig. 1 is a diagrammatic, cross-sectional view of a pair of fragments of a semiconductor construction shown at a preliminary processing step of a method of the present invention.

[0012] Fig. 2 is a view of the Fig. 1 fragments shown at a processing step subsequent to that of Fig. 1.

[0013] Fig. 3 is a view of the Fig. 1 fragments shown at a processing step subsequent to that of Fig. 2.

[0014] Fig. 4 is a view of the Fig. 1 fragments shown at a processing step subsequent to that of Fig. 3.

[0015] Fig. 5 is a view of the Fig. 1 fragments shown at a processing step subsequent to that of Fig. 4.

[0016] Fig. 6 is a view of the Fig. 1 fragments shown at a processing step subsequent to that of Fig. 5.

[0017] Fig. 7 is a view of a pair of semiconductor wafer fragments shown at a preliminary processing step of a second method of the invention.

[0018] Fig. 8 is a view of the Fig. 7 fragments shown at a processing step subsequent to that of Fig. 7.

[0019] Fig. 9 is a view of the Fig. 7 fragments shown at a processing step subsequent to that of Fig. 8.

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[0020] Fig. 10 is a diagrammatic, cross-sectional view of an apparatus which can be utilized for treating a semiconductor construction in accordance with an embodiment of the present invention.

[0021] Fig. 11 is a view of an apparatus which can be utilized for treating a semiconductor construction in accordance with an embodiment of the present invention different from the embodiment illustrated in Fig. 10.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

[0023] A first embodiment of the invention is described with reference to Figs. 1-6. Referring to Fig. 1, a pair of fragments of a semiconductor construction 10 are illustrated. Such fragments are labeled as 12 and 14. Referring initially to fragment 12, such comprises a semiconductive material substrate 16 doped to n-type with conductivity-enhancing dopant. Substrate 16 can comprise, for example, monocrystalline silicon. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers

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to any supporting structure, including, but not limited to, the semiconductive substrates described above.

[0024] A pair of isolation regions 18 are formed within substrate 16, and can be formed utilizing, for example, shallow trench isolation methodologies. A layer 20 of silicon dioxide is formed across an upper surface of substrate 16. Layer 20 has an upper surface 22 which can be referred to herein as a first silicon-comprising surface.

[0025] Referring next to fragment 14, such comprises a substrate 26. Substrate 26 can comprise the monocrystalline silicon material of substrate 16, but is doped to a p-type with conductivity-enhancing dopant. A pair of isolation regions 28 are formed over substrate 26, and a silicon dioxide layer 30 is formed across an upper surface of substrate 26 between the isolation regions 28. Isolation regions 28 and silicon dioxide layer 30 can comprise identical constructions to those discussed previously with respect to isolation regions 18 and silicon dioxide layer 20. Silicon dioxide layer 30 has an upper surface 32 which can be referred to herein as a second silicon-comprising surface.

[0026] Fragments 12 and 14 can be utilized for forming a PMOS transistor structure and an NMOS transistor structure, respectively; and can ultimately be incorporated into a CMOS assembly.

[0027] Referring to Fig. 2, surfaces 22 and 32 are exposed to activated nitrogen 40 to form nitrogen-comprising layers 42 and 44. Specifically, the activated nitrogen 40 can interact with silicon of the silicon-comprising surfaces to form a new material comprising silicon and nitrogen which defines layers 42 and 44. If silicon-comprising surfaces

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22 and 32 initially comprise silicon dioxide, layers 42 and 44 can comprise compositions of silicon, oxygen and nitrogen. It is noted that the invention encompasses embodiments (not shown) wherein silicon dioxide layer 20 is omitted, and wherein an upper surface of substrate 16 is exposed to the activated nitrogen. If substrate 16 consists of or consists essentially of silicon, the nitrogen-containing layer formed from an upper surface of substrate 16 can comprise, consist of or consist essentially of silicon nitride.

[0028] Layers 42 and 44 are preferably formed to a thickness of from about 5Å to about 10Å. The layers are formed by exposing surfaces 22 and 32 to the activated nitrogen 40 for a desired power/time combination. Such power/time combination preferably includes a time of at least about 20 seconds; with the preferred time being from about 20 seconds to about 5 minutes; and a more preferred time being at least about 40 seconds. The activated nitrogen 40 is formed by exposing a nitrogen precursor (such as, for example, N_2) to a plasma maintained at a power of the power/time combination of at least about 1,500 watts, and preferably of from about 750 watts to about 5,000 watts. Surfaces 22 and 32 are preferably maintained at temperatures of from about 25°C to about 400°C during the exposure of such surfaces to the activated nitrogen. Such can be accomplished by maintaining an entirety of wafer 10 at the desired temperature of from about 25°C to about 400°C during the exposure of surfaces 22 and 32 to the activated nitrogen. The activated nitrogen treatment can occur in a reaction chamber, with a pressure in the chamber being maintained

at from about 1 mTorr to about 1 Torr during the treatment. The activated nitrogen treatment can be followed by an anneal at, for example, about 900°C for a time of from about 10 seconds to about two minutes, an preferably for about 60 seconds. The anneal temperature can be attained through rapid thermal processing (RTP) with a ramp rate of at least about 10°C/sec.

[0029] The activated nitrogen utilized in methodology of the present invention is formed by exposing surfaces 22 and 32 to high-power generated activated nitrogen for longer durations than occur in prior art processes. It is noted that the combination of power and duration separates activated nitrogen exposure of the present invention from prior art processes. Specifically, if a low-power generated activated nitrogen species is utilized for a long duration exposure, such can be substantially equivalent to utilization of a high-power generated activated nitrogen species for a short duration exposure. However, the present invention utilizes high-power generated activated nitrogen in combination with a long duration exposure to preferably form a peak nitrogen concentration of at least about 15%; which far exceeds the nitrogen concentration utilized to in prior art processes prevent dopant (e.g., boron) penetration. The present invention is thus different than the prior art processes that have been utilized for forming dielectric materials of transistor gates to prevent dopant penetration. The combination of the high power plasma generation of activated nitrogen together with the long duration exposure of surfaces 22 and 32 to the activated nitrogen forms a nitrogen-containing layer 42 which is suitable for a desired purpose of

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reducing a dopant concentration of a V_t implant for a PMOS device. Prior art processing did not utilize the high plasma power in combination with the long-duration exposure of the present invention because the prior art was attempting to obtain a different result from the silicon/nitrogen-containing layers formed by such methodologies. Accordingly, the present methodologies were not considered appropriate for the prior art purposes described in the "Background" section of this disclosure.

[0030] Figs. 10 and 11 diagrammatically illustrate processing which can be utilized for generating and utilizing the activated nitrogen species 40. It is to be understood that other processing, and other reaction chambers besides the designs illustrated in Figs. 10 and 11 can be utilized in embodiments of the present invention.

[0031] Referring initially to Fig. 10, such illustrates an apparatus 100 comprising a reaction chamber 102 surrounded by coils 104. Coils 104 are ultimately utilized for providing power within chamber 102 to maintain a plasma 106. Coils 104 can, for example, be utilized to provide radio frequency (Rf) power.

[0032] Wafer 10 is illustrated supported upon a holder 108. A cooling mechanism (not shown) can be provided to cool a back surface of wafer 10 and accordingly hold the upper (treated) surface of wafer 10 at the desired temperature of from about 100°C to about 400°C by cooling an entirety of the wafer 10.

[0033] Nitrogen-comprising precursor (such as, for example, N_2) is flowed into chamber 102 through appropriate ports (not shown) to form

activated nitrogen. In the shown embodiment, the glow of plasma 106 is not in contact with a treated surface of wafer 10, and accordingly plasma 106 can be considered to be remote relative to the treated surface of wafer 10. Activated nitrogen exits glow 106, and some of the activated nitrogen can ultimately migrate to an upper surface of wafer 10 to treat such upper surface (with the migration of the activated nitrogen being indicated by arrows pointing downwardly from plasma 106 to wafer 10).

[0034] Referring to Fig. 11, a different embodiment apparatus 120 is illustrated diagrammatically. Apparatus 120 comprises a reaction chamber 122 surrounded by coils 124. Coils 124 can be utilized to provide power to a plasma 126. Wafer 10 is illustrated within chamber 122 and is shown supported on a holder 128. Wafer 10 can be cooled in chamber 122 by a cooling mechanism (not shown) similar to that described previously with respect to the apparatus 100.

[0035] A difference between the embodiment of Fig. 11 and that of Fig. 10 is that the plasma glow 126 of Fig. 11 contacts the treated surface of wafer 10. Accordingly, activated nitrogen species can be formed in direct contact with the treated surface of wafer 10. The process illustrated in Fig. 11 can be referred to as direct plasma nitridation, in that the activated nitrogen species can be formed in direct contact with the treated surface.

[0036] The activated nitrogen species formed within apparatus 120 can be generated by flowing a nitrogen precursor (such as, for example, N_2) into reaction chamber 122 through appropriate ports (not shown).

[0037] Referring to Fig. 3, wafer fragments 12 and 14 are illustrated after a V_t implant has been provided at an upper surface of the substrate regions 16 and 26. The V_t implant within fragment 12 is labeled as 50 and that within fragment 14 is labeled as 52. It is noted that the V_t implant 52 would typically comprise different dopants and concentrations than 50; and accordingly region 14 would typically be masked during formation of implant 50, while region 12 would typically be masked during formation of implant 52. Also, it is noted that even though the V_t implants are shown at the processing step of Fig. 3, it is to be understood that such implants can be formed at a different processing step, such as, for example, the processing step of Fig. 1, by implanting suitable conductivity-enhancing dopants through dielectric layers 28 and 30. In the embodiment of Fig. 3, the suitable conductivity-enhancing dopants have been implanted through dielectric materials 20 and 30, as well as through nitrogen-containing layers 42 and 44.

[0038] Implant region 50 will ultimately be incorporated into a PMOS transistor device, and can advantageously have a dopant concentration of less than 7×10^{17} atoms/cm^3; preferably less than 5×10^{17} atoms/cm^3; and can, for example, have the dopant concentration within a range of from about 1×10^{17} atoms/cm^3 to about 7×10^{17} atoms/cm^3, or a range of from about 1×10^{17} atoms/cm^3 to about 5×10^{17} atoms/cm^3. The utilization of the relatively low concentration of conductivity-enhancing dopant for V_t implant region 50 is possible because of the nitrogen-containing layer 42. Specifically, nitrogen-containing layer 42 enables a PMOS transistor to be formed with a

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lower concentration V_t implant, and still have the desired electrical properties which previously could be accomplished only with higher concentrations of V_t implants. A possible mechanism by which the nitrogen of nitrogen-containing layer 42 reduces a desired level of dopant in a PMOS device is by affecting donor-type interface states. Such mechanism is presented herein to assist the reader in understanding the invention, and is not to be utilized in limiting the invention. Due to the expected affect of the of the nitrogen on donor-type interface states, it is also expected that the nitrogen will have little, if any, affect on the desired V_t dopant concentration of an NMOS device. Such expectation is consistent with actual findings.

[0039] In the shown embodiment, the V_t implant 52 is ultimately incorporated into an NMOS device, and, as mentioned above, the concentration of conductivity-enhancing dopant in such V_t implant is generally largely unaffected by nitrogen-comprising layer 44. Accordingly, V_t implant region 52 will have about the same concentration of conductivity-enhancing dopant as would a prior art V_t implant provided for an NMOS device. Although nitrogen-comprising layer 44 has not provided advantages relative to a concentration of dopant utilized in V_t implant region 52, layer 44 can provide other advantages for an NMOS device. Specifically, layer 44 can reduce an effective thickness of dielectric material required to achieve a particular dielectric strength. Specifically, nitrogen-comprising layer 44 will typically have a different dielectric constant than material 30, and accordingly the relative thicknesses of materials 30 and 44 can influence the dielectric strength

of the mass comprising layers 30 and 44. Accordingly, variation of the relative thickness of layer 44 to layer 30 can be utilized as a parameter for controlling the dielectric strength of the mass comprising layers 30 and 44.

[0040] In particular embodiments, it can be desired to avoid formation of a nitrogen-comprising layer over NMOS region 14. In such embodiments, region 14 can be masked during formation of the nitrogen-comprising layer over PMOS region 12. An exemplary procedure which can be incorporated into such embodiments is described below with reference to Figs. 7-9.

[0041] Referring to Fig. 4, conductive transistor gate materials 54, 56 and 58 are formed over region 12; and conductive gate materials 60, 62 and 64 are formed over region 14. Materials 54, 56 and 58 can comprise, for example, conductively-doped silicon (such as silicon conductively doped with p-type conductivity-enhancing dopant); metal silicide (for example, tungsten silicide or titanium silicide); and metal (for example, tungsten or titanium).

[0042] Layers 60, 62 and 64 can comprise, for example, conductively-doped silicon, silicide and metal, respectively. Layer 60 can comprise, for example, conductively doped polycrystalline silicon, and in particular applications can comprise n-type doped silicon; silicide 62 can comprise, for example, tungsten silicide or titanium silicide; and metal 64 can comprise, for example, tungsten or titanium.

[0043] Insulative layers 66 and 68 are formed over the conductive transistor gate layers. Layers 66 and 68 can comprise, for example,

silicon nitride or silicon dioxide, and in particular applications can comprise identical compositions as one another. Also, it is noted that layer 60, 62 and 64 can, in particular applications, comprise identical constructions as layers 54, 56 and 58, respectively.

[0044] Referring to Fig. 5, layers 20, 42, 54, 56, 58 and 66 are patterned into a first stack 70; and layers 30, 44, 60, 62, 64 and 68 are patterned into a second stack 72. The patterning of stacks 70 and 72 can be accomplished by, for example, forming a layer of photoresist (not shown) over layers 66 and 68; photolithographically patterning the photoresist; transferring a pattern from the photoresist to the underlying materials with a suitable etch; and subsequently removing the photoresist.

[0045] Stack 70 comprises a first transistor gate which includes patterned conductive layers 54, 56 and 58; and stack 72 comprises a second transistor gate which includes patterned conductive layers 60, 62 and 64. The first transistor gate defines a first channel region 74 thereunder, and second transistor gate defines a second channel region 76 thereunder. The transistor gates are separated from the channel regions by dielectric material. Specifically, the first transistor gate is separated from the first channel region 74 by patterned dielectric materials 20 and 42; and the second transistor gate is separated from the second channel region 76 by patterned dielectric materials 30 and 44.

[0046] Referring to Fig. 6, sidewall spacers 80 are provided laterally adjacent first stack 70; and sidewall spacers 82 are provided laterally adjacent second stack 72. Sidewall spacers 80 and 82 can be formed

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from, for example, either silicon nitride or silicon dioxide. The sidewall spacers can be formed by, for example, providing a layer of suitable material over wafer 10, and subsequently anisotropically etching the material to leave sidewall spacers 80 and 82 remaining.

[0047] A first pair of source/drain regions 84 are provided within substrate 16, and provided to be spaced from one another by channel region 74. Source/drain regions 84 comprise a heavily doped portion 83 and a lightly doped portion 85. Heavily doped portion 83 will be heavily doped with p-type conductivity-enhancing dopant. Regions 85 and 83 can be formed by conventional methods. A second pair of source/drain regions 86 are provided within substrate 26, and provided to be spaced from one another by channel region 76. Source/drain regions 86 comprise heavily-doped regions 87 and lightly doped regions 89. Regions 87 will be heavily doped with n-type conductivity-enhancing dopant. Regions 87 and 89 can be formed by conventional processing.

[0048] The stack 70, together with source/drain regions 84 and channel regions 74, defines a PMOS transistor construction 90; and the stack 72 together with source/drain regions 86 and channel region 76 defines an NMOS transistor construction 92.

[0049] A second embodiment method of the present invention is described with reference to Figs. 7-9. Referring to Fig. 7, two fragments 202 and 204 of a wafer 200 are illustrated. Fragment 202 comprises a substrate 206 having a dielectric material layer 208 thereover. Substrate 206 can comprise, for example, monocrystalline silicon, and can be either majority n-type doped or majority p-type

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doped. A pair of isolation regions 210 are supported by substrate 206. Isolation regions 210 and dielectric layer 208 can comprise constructions identical to those described above with reference to isolation regions 18 and dielectric layer 20 of Fig. 1. A masking material 212 is formed over substrate 206, and covers an upper surface of fragment 202. Masking material 212 can comprise, for example, photoresist, and can be patterned by photolithographic processing. Fragment 202 will ultimately be utilized for formation of a transistor structure, and accordingly a first channel region location 214 is defined within substrate 206.

[0050] Fragment 204 comprises the substrate 206. The substrate 206 can be majority doped with the same dopant type in fragment 204 as utilized in fragment 202, or alternatively substrate 206 can comprise a different majority dopant type in fragment 204 than in fragment 202. In particular aspects of the present invention, substrate 206 will comprise p-type background doping in fragment 202 so that an NMOS transistor can be formed relative to fragment 202, and substrate 206 will comprise n-type background doping in fragment 204 so that a PMOS transistor can be formed relative to fragment 204. In other embodiments, substrate 206 will comprise majority n-type doping in both fragments 202 and 204 so that PMOS transistors are ultimately formed relative to both of fragments 202 and 204.

[0051] A pair of isolation regions 216 are formed relative to fragment 204, and a dielectric material 218 is formed across an upper surface of substrate 206 and between isolation regions 216. A second

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channel region location 220 is defined beneath dielectric material 218, and will ultimately be incorporated into a second transistor structure.

[0052] Wafer 200 is shown exposed to activated nitrogen 222. Masking layer 212 protects an upper surface of fragment 202 from the activated nitrogen, whereas an upper surface of fragment 204 is exposed to the activated nitrogen 222 to form a nitrogen-comprising layer 224 across fragment 204. Activated nitrogen 222 can be formed utilizing conditions similar to those discussed previously with reference to Fig. 2. Specifically, wafer 200 can be held at the same conditions described previously with reference to Fig. 2, and exposed to activated nitrogen 222 for the same duration of time as described previously with reference to Fig. 2.

[0053] Referring to Fig. 8, masking layer 212 (Fig. 7) is removed and V_t implants 226 and 228 are formed relative to fragments 202 and 204, respectively. V_t implant 228 can be different than implant 226, and can, for example, be formed while masking 212 is in place over fragment 202. Also, a separate mask (not shown) can be provided over fragment 204 while V_t implant 226 is formed within fragment 202. In embodiments in which substrate 206 comprises n-type majority doping relative to both fragments 202 and 204, and accordingly wherein PMOS devices are to ultimately be formed relative to both of the fragments, V_t implant 228 can be formed to a lower concentration of conductivity enhancing dopant than is V_t implant 226.

[0054] Conductive transistor gate materials 230, 232 and 234 are formed relative to fragment 202; and conductive transistor gate materials

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236, 238 and 240 are formed relative to fragment 204. Materials 230, 232 and 234 can comprise, for example, conductively doped silicon, metal silicide and metal, respectively; and materials 236, 238 and 240 can similarly comprise conductively doped silicon, metal silicide and metal, respectively. The conductively doped silicon layers 230 and 236 can comprise either n-type or p-type doped silicon, such as, for example, conductively doped polycrystalline silicon. The metal silicide layers 232 and 238 can comprise, for example, titanium silicide or tungsten silicide. The metal layers 234 and 240 can comprise, for example, titanium or tungsten.

[0055] If fragments 202 and 204 are both being utilized for forming PMOS transistors, the layers 232 and 236 can be identical to one another and formed in a common processing step; the layers 232 and 238 can be identical to one another and formed in the same processing step; and the layers 234 and 240 can be identical to one another and formed in the same processing step. Also, if layers 202 and 204 are to be utilized for forming a PMOS transistor and an NMOS transistor, respectively; the layers 232 and 238 can be identical and formed in the same processing step, and the layers 234 and 240 can be identical and formed in the same processing step. If layers 202 and 204 are to be utilized for forming a PMOS transistor and an NMOS transistor, respectfully; the layers 230 and 236 can be identical and formed in the same processing step, or the layers 230 and 236 can be different in comprising a different type of conductivity dopant relative to one another.

[0056] An insulative material 242 is formed over conductive material 234, and an insulative material 244 is formed over conductive material 240. Insulative materials 242 and 244 can comprise the same composition as one another, and can be formed in the same processing step. Exemplary materials for layers 242 and 244 are silicon dioxide and silicon nitride.

[0057] Referring to Fig. 9, layers 208, 230, 232, 234 and 242 are patterned into a stack 250; and layers 218, 224, 236, 238, 240 and 244 are patterned into a second stack 252. Stacks 250 and 252 comprise transistor gate constructions, and accordingly define channel regions therebeneath. Such channel regions are in channel region locations 214 and 220, respectively.

[0058] Sidewall spacers 260 are formed adjacent stack 250, and sidewall spacers 262 are formed adjacent stack 252. Sidewall spacers 260 and 262 can comprise constructions identical to those discussed above for sidewall spacers 80 and 82 of Fig. 6.

[0059] A pair of source/drain regions 264 are provided relative to stack 250 and spaced from one another by the channel region at location 214; and a pair of source/drain regions 270 are provided relative to stack 252 and spaced from one another by the channel region at location 220. Source/drain regions 264 comprise a heavily doped region 263 and a lightly doped region 265, whereas source/drain regions 270 comprise a heavily doped region 269 and a lightly doped region 271.

[0060] A first transistor structure 290 is defined by stack 250 in combination with source/drain regions 264; and a second transistor 300

is defined by stack 252 in combination with source/drain regions 270. In embodiments in which both of transistor structures 290 and 300 comprise PMOS transistors, the transistor construction 300 can have a different V_t doping than does the transistor construction 290. Such can enable transistor structure 300 to be tailored for a different purpose than transistor structure 290. For instance, in embodiments in which transistor structures 290 and 300 are utilized for logic circuitry, it can be desirable to have one set of transistors with different operating characteristics than another set. Utilization of nitrogen-containing layer 224 in combination with tailored V_t doping of region 228 can enable transistor construction 300 to be specifically tailored for suitability for different operations than transistor structure 290. In alternative embodiments in which transistor structure 290 corresponds to an NMOS transistor and transistor structure 300 corresponds to a PMOS transistor, it can be advantageous to leave the nitrogen-containing layer (224) out of the NMOS transistor construction.

[0061] Transistor constructions 290 and 300 can be considered to define two separate groups of transistor constructions, with transistor construction 290 corresponding to a group which is covered during formation of the nitrogen-comprising layer (224), and which accordingly does not comprise such nitrogen-comprising layer. In contrast, the group corresponding to transistor construction 300 does comprise the nitrogen-comprising layer 224.

[0062] In compliance with the statute, the invention has been described in language more or less specific as to structural and

methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

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